REMARKS

Claims 1-3 are pending. The Examiner sustained his objections to the drawings and specification, along with his rejections of the claims. Each of these objections and rejections have been obviated by argument and/or amendment as described in the following sections. Accordingly, Applicant respectfully requests that the Examiner withdraw the objections and rejections and issue a Notice of Allowance for claims 1-3.

A. Drawing Objections

The Examiner sustains the objection to the drawings as not showing every claimed feature pursuant to 37 CFR 1.83(a). IN particular, the Examiner objects to a "solder-containing compound" not being shown. In response to this objection, Applicant has submitted a proposed drawing change to add Fig. 12, which is a flow diagram that discloses a method for making an integrated circuit stack module according to one embodiment of the invention. Claims 1 through 3 are process (or method) claims. As such, the flow diagram of Fig. 12, which recites the act of applying a solder-containing compound to a plurality of members at steps 62 and 65. This flow diagram satisfies the provision of Rule 1.81(b), which states that, "drawings may include illustrations which facilitate an understanding of the invention (for example, flow-sheets in cases of processes, and diagrammatic views)." (See 37 CFR 1.181(b)). Accordingly, it is urged that the drawing objection be withdrawn.

B. Specification Objections

The Examiner objects to the specification because it is not clear that it provides antecedent basis for the claim term: "plural iterations." To expedite prosecution, in response to this objection, Applicant has amended the claims to remove this term. In particular, claim 2 has been amended to recite "in which the carrier frame is provided from a carrier bed having a

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plurality of carrier frames" rather than "in which plural iterations of the carrier frame are created in a carrier bed." This change is fully supported by Fig. 11 and the accompanying description in the specification. Thus, it is urged that this objection be withdrawn.

C. Section 112 Claim Rejections

The Examiner rejected claims 1-3 as being indefinite under 35 U.S.C. 112, second paragraph. Claim 1 is rejected because it is unclear whether the term, "solder-containing compound" as recited in the second and fifth steps are the same. In response to this rejection, Applicant has amended claim 1 to now recite: "applying a first portion of a solder-containing compound . . ." and "applying a second portion of the solder-containing compound . . ." This should make it clear that separate portions of a solder-containing compound are applied to the first and second sides of the plurality of members.

Similarly, the Examiner found the use of the term: "solder connections" in both the third and sixth steps to be unclear as to whether or not they are the same. In response to this rejection, Applicant has amended claim 1 to recite "a first set of solder connections . . ." in the third claim step and "a second set of solder connections . . ." in the sixth claim step to clarify that they are not the same connections.

Finally, the Examiner found the term "plural iterations" in claim 2 to be relative and unclear. As noted above with regard to the specification objection, Applicant has removed this term from the claims. Thus, the claims are now clear pursuant to the second paragraph of Section 112, and it is requested that the rejections be withdrawn.

D. Section 103 Claim Rejections

The Examiner sustained his rejections of claims 1-3 as being obvious over Hikita (U.S. Pat. No. 6,133,637) in view of Sakai (U.S. Pat. No. 5,894,984). The Examiner points out that

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Hikita at col. 5, ll. 10-11 teaches applying a solder-containing compound (14C)to the sides of a plurality of members; at Figs. 43-45, it teaches placing packaged integrated circuits (14, 16) on the contact members; and at col. 21, ll. 12-14 and Figs. 43-45, it teaches processing the packaged integrated circuits and the carrier frame using transfer molding to make solder connections between the integrated circuits and the contact members. From this, the Examiner contends that Hikita teaches the claimed method of claim 1 except that it doesn't directly teach processing the IC and frame members by heating them. Sakai, at Fig. 8 and col. 1, ll. 24-33, is presented to fill this gap as it teaches the act of using heat in a transfer molding step. The Examiner thereby asserts that Hikita and Sakai disclose Applicant's claimed method of making a stacked module of packaged integrated circuit devices (hereinafter, "ICs"). Applicant traverses this rejection because in fact, Hikita and Sakai—either alone or in combination—do not teach Applicant's claimed method.

Contrary to the Examiner's assertion, Hikita does not teach processing ICs with carrier frame contact members to create solder connections between the ICs and their associated side of the plurality of contact members, as is recited in claim 1. The Examiner points to col. 5, ll. 10-11 as teaching the solder-containing compound (14C) limitation. This excerpt describes the stacked module shown in Figure 2. Applicant agrees that solder bumps (14c) are taught, but they do not connect the ICs (14, 16) to frame contact members (12b). Rather, they connect IC electrode pads (14a, 16a) to one another and not to the frame members (12b). As best seen in Fig. 4, the frame contact members (12b) are actually connected to the IC electrode pads via bonding wires W. Likewise, the embodiment taught in Figs. 43-45 and at col. 21, ll. 12-14 also does not teach solder connections connecting ICs to different sides of a plurality of frame contact members. In this embodiment, frame contacts 12b are sandwiched between the upper and lower ICs, but the

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IC electrode pads (and the ICs) are not connected to the contact members using solder connections. Rather, they are connected through an anisotropic conductive film in combination with solder. Thus, the connections are not solder connections but instead are conductive film/solder connections.

The solder bumps (14c) connect the electrode pads to the anisotropic conductive film (24), which in turn are connected to the frame contacts (12b). From Hikita, the solder bumps (14c) can be applied to the frame member contacts (12b) or alternatively to both the electrode pads (14a, 16b) and the frame contacts, but the conductive film (24) is always interposed within the IC electrode pads, the solder bumps, and the frame contact members. Therefore, Hikita does not teach solder connecting the ICs to the frame contacts, as is required by the pending claims. It is worth pointing out that the use of the anisotropic conductive film (24) is not trivial. Anisotropic conductive films allow current to only conduct in one axis, i.e., in the Z-axis between the electrode pads and the over or underlying contact members.[1] In other words, they inhibit current from flowing laterally between adjacent pads or adjacent contact members, which serves to prevent undesirable shorting. Accordingly, for their use to be most effective, solder should be avoided on either or even both sides of the conductive film. In fact, Hikita states that "the [solder] bumps 14c and 16b may be omitted and the conductive films 24a and 24b be partially compressed and deformed only by the lead terminals 12b." (Hikita col. 21, ll. 28-30). Therefore, Hikita does not teach the "processing" steps of claim 1 because it does not teach the creation of solder connections between the contact members and IC devices.

[1] In a published glossary by the Technical Knowledge Base (at http://www.tkb-4u.com/glossarylist/glossary_in.php), anisotropic conductive adhesive is defined as: "conductive adhesives that conduct electricity in one direction only. Also referred to as 'Z-axis conductive adhesives.' When using this type of adhesive, high Z-axis forces are required during bonding. Components attached using this material use the pick, place, and attach process."

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Furthermore, Hikita's ICs (14, 16) are not packaged when connected to their lead frame sides, pursuant to and as required by the third and sixth steps of claim 1. This is evidenced by the fact that Hikita teaches using transfer molding to package the assembly with an epoxy or resin after the ICs are connected to the lead frame. In one published technical glossary, the term "package" is defined as follows:

> The protective container or housing for an electronic component or die, with external terminals to provide electrical access to the components inside.

(See Intersil's Glossary of Semiconductor Terms at http://rel.intersil.com/docs/lexicon/P.html). From this definition, the ICs (14, 16) are clearly not packaged until the entire module is "packaged" in a resin or epoxy through transfer molding with the external lead frame leads (12b) providing connectivity to the interior ICs. This "packaged" limitation is not unimportant. Applicant's inventive method allows for off-the-shelf, packaged ICs, old or new, to be stacked in a reliable, effective manner. Neither Hikita nor Sakai teach anything with this capability.

Accordingly, Applicant's claims are not obvious over Hikita and Sakai. A Notice of Allowance is thereby respectfully requested.

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CONCLUSION

Applicant believes the claims to be patentable over the cited prior art. If the Examiner has any questions or concerns whatsoever, he is encouraged to immediately contact Erik Nordstrom at 512/238-7253.

via facsimile

Respectfully submitted,

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